AMENDMENTS TO THE CLAIMS

In the Claims:

1. (Currently amended) A clock distortion detector, comprising:

an input for receiving a first clock signal;

a second input for receiving a second clock signal;

a first mirror delay element comprising at least one input, at least one output, and at least one control input;

and a second mirror delay element comprising at least one input, at least one output, and at least one control input, wherein the output of the first mirror delay element is coupled to the input of the second mirror delay element, and the output of the second mirror delay element is coupled to the input of the first mirror delay element, and the control input of the first mirror delay element and the control input of the second mirror delay are coupled to the input of the clock distortion detector for receiving the first signal.

2. (Canceled)

3. (Previously Presented) The clock distortion detector of claim 1, wherein the first and the second mirror delay elements are synchronous mirror delay elements.

4. (Previously Presented) The clock distortion detector of claim 1, wherein the first and the second mirror delay elements each additionally comprises two control inputs.

5. (Original) The clock distortion detector of claim 4, wherein the first clock signal is fed to the respective first control inputs, and the second clock signal is fed to the respective second control inputs.

6. (Original) The clock distortion detector of claim 5, wherein the first and the second mirror delay elements are synchronous mirror delay elements.

7. (Previously Presented) The clock distortion detector of claim 1, further comprising a test device coupled to the input of the first mirror delay element.

8. (Original) The clock distortion detector of claim 7, wherein the test device additionally is coupled to the output of the first mirror delay element.

9. (Original) The clock distortion detector of claim 8, wherein the test device is configured to compare the signal input into the first input of the first mirror delay element with a signal output at the output of the first mirror delay element.

10. (Original) A clock distortion detection method, comprising:

applying a clock signal to a control input of a first mirror delay element; and

applying the clock signal to a control input of a second mirror delay element,

wherein a signal output by the first mirror delay element is applied to the second mirror delay element, and

a signal output by the second mirror delay element is applied to the first mirror delay element.

11. (Previously Presented) A clock distortion detector, comprising:

a first input for receiving a first clock signal;

a second input for receiving a second clock signal;

at least one mirror delay element;

a first mirror delay element, comprising two inputs and two outputs; and

a second mirror delay element, comprising two inputs and two outputs,

wherein a second output of the first mirror delay element is coupled with a first input of the second mirror delay element, and

a first output of the second mirror delay element is coupled with a second input of the first mirror delay element.

12. (Previously Presented) The clock distortion detector of claim 11, wherein the first and the second mirror delay elements are synchronous mirror delay elements.

13. (Previously Presented) The clock distortion detector of claim 11, wherein the first and the second mirror delay elements each additionally comprise two control inputs.

14. (Previously Presented) The clock distortion detector of claim 13, wherein the first clock signal is fed to the respective first control inputs, and the second clock signal is fed to the respective second control inputs.

15. (Previously Presented) The clock distortion detector of claim 14, wherein the first and the second mirror delay elements are synchronous mirror delay elements.

16. (Previously Presented) The clock distortion detector of claim 11, further comprising a test device coupled to a first input of the first mirror delay element.

17. (Previously Presented) The clock distortion detector of claim 16, wherein the test device additionally is coupled to a first output of the first mirror delay element.

18. (Previously Presented) The clock distortion detector of claim 17, wherein the test device is configured to compare the signal input into the input of the first mirror delay element with a signal output at the first output of the first mirror delay element.